REMARKS

Claims 1 and 12 have been amended for clarity. Claims 1-22 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 102(b) Rejection:

The Office Action rejected claims 1, 3-12 and 14-21 under 35 U.S.C. § 102(b) as being anticipated by Budelman (U.S. Patent 5,629,608). As set forth in more detail below, Applicants respectfully traverse this rejection.

Amended claim 1 states in pertinent part "wherein one of the components is a switching regulator; ... wherein the switching regulator is configured to regulate the supply voltage and to provide a termination voltage, separate from the supply voltage, to the system memory". Amended claim 12 includes similar language in pertinent part.

The Office Action asserts that Budelman's item 450 of Fig. 4 is equivalent to the switching regulator of claim 1. However, at col. 4, lines 63-65 Budelman describes item 450 of figure 4 as "a linear load element coupled to the output of the voltage regulating device to help sink excess current". This description does not describe a switching regulator that provides a termination voltage. As an example of load 450, Budelman's figure 7 shows a FET 750, and col. 7, lines 14-16 states: "The linear load 750 operates to sink excess current". A single FET cannot function as a switching regulator, and therefore, Budelman's load 450 cannot be the switching regulator of claim 1. Budelman's load 450 clearly does not supply a termination voltage. Instead, Budelman's load 450 is simply a linear load that can be selectively applied to the output of regulators 420 and 440.

Furthermore, Budelman does not teach that the switching regulator provides a termination voltage separate from the supply voltage regulated by the switching

regulator, as recited in claims 1. Budelman's regulator provides only a single supply voltage, as illustrated in Figures 3, 4, and 7, whereas the switching regulator of claim 1 provides "a termination voltage, separate from the supply voltage, to the system memory". Therefore, Budelman does not anticipate claim 1 or claim 12.

With regard to claims 3 and 15 the Office Action asserts that Budelman's window reference circuit (735 of Fig. 7) is equivalent to the detecting stage of the cited claims and that the window reference circuit is a voltage divider connected to the supply voltage. First, Budelman's window reference circuit is at no point connected to the supply voltage. It is connected to a constant reference voltage, $+V_{REF}$, as shown in figure 7. Second, Budelman's window reference circuit provides two constant reference voltages to which a varying supply voltage is compared. Conversely, the voltage divider of claims 3 and 15 provides a scaled version of a varying supply voltage for comparison with a constant reference. Therefore, Budelman's window reference circuit cannot be the voltage divider of claims 3 and 15. Budelman does not teach the combination of features recited in claims 3 and 15, and Applicants respectfully traverse this rejection.

With regard to claim 21 the Office Action attempts to apply the incorrect component equivalence from its argument with regard to claims 3 and 15 to the limitations of claim 21. This results, at best, in Budelman's circuit functioning in a manner exactly opposite to that described by the Office Action regarding claim 21. The Office Action asserts that Budelman's window reference circuit 735 applies an input voltage to his comparator circuitry 740. The Office Action then asserts "the input voltage is greater than or equal to a reference voltage of the shunt regulator when the voltage on the voltage rail is greater than or equal to a first voltage level. . . wherein the shunt regulator turns on when the input voltage is greater than or equal to the reference voltage". This assertion is inconsistent with Budelman's circuit of Figure 7. First, the input voltage from Budelman's window reference circuit 735 is applied to the negative input of comparator 742. The only mechanism for turning on Budelman's load 750 is a positive output from comparator 742, which only occurs when its positive input is at a higher voltage level than its negative input. These assertions force the equivalence of the

reference voltage and the supply voltage, which is tied to the positive input of the comparator. Therefore, when the input voltage is greater than or equal to the reference voltage, the output of the comparator will in point of fact be low causing the load to be off, which is directly contradictory to the assertion of the Office Action. Therefore, Budelman's circuit of figure 7 cannot be the clamping circuit of claim 21.

Furthermore, as discussed above in regard to claim 3, the voltage divider in Fig. 7 of Budelman is coupled to a reference voltage $+V_{REF}$, not the voltage rail being clamped, as recited in claim 21. Thus, claim 21 is clearly not anticipated by Budelman.

The dependent claims are patentable for at least the reasons given above in regard to their respective independent claims, although Applicants reserve the right to present additional arguments in regard to any of the claims should it become necessary at a later date.

Section 103(a) Rejections:

The Office Action rejected claims 2 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Budelman in view of Lee, et al. (U.S. Patent 5,920,511) (hereinafter "Lee"). Applicants respectfully traverse this rejection in light of the following remarks.

With regard to claims 2 and 13, neither Budelman nor Lee, either alone or in combination, teach or suggest the claimed system. Lee does divulge the existence of DDR-SDRAM, but is completely silent on powering such devices. As was pointed out with regard to claim 1, Budelman says nothing about providing "a termination voltage, separate from the supply voltage, to the system memory" that is limited to DDR SDRAM by claim 2. Thus, Applicants respectfully traverse the rejection.

Claim 22 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Budelman in view of Taylor (U.S. Patent 5,834,958). Claim 22 depends from claim 21 and is therefore patentable for at least the reasons given with regard to claim 21.

Furthermore, the circuit in Taylor including resistor R3 is completely different from the circuit of Fig. 7 in Budelman. The use of R3 in Taylor does not suggest adding a resistor between the comparator and FET in Budelman.

CONCLUSION

Applicants submit the application is in condition for allowance, and notice to that effect is requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicants hereby petition for such extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/5500-64600/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

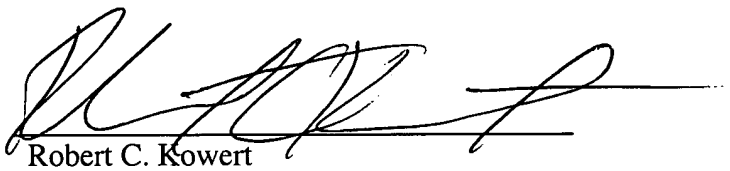
☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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